DESIGN OF LOW POWER REVERSIBLE MULTIPLIER

MADHINA BASHA, ARNNPALLI JAYA PRAKASH & KARUKOLA GIRIJA

Department of Electronics and Communication, VITS Group of Institutions, Visakhapatnam, Andhra Pradesh, India

ABSTRACT

Reversible computing is a promising alternative to these technologies, with applications in ultra-low power, nano computing, quantum computing, low power CMOS design, optical information processing, bioinformatics etc. In reversible logic the power dissipation can be minimized or even eliminated. Power dissipation is one of the most important factor in the VLSI circuits design .In this paper a 4x4 reversible multiplier circuit is proposed with the design of two new reversible gates called ABC and GPS gates. In this paper the reversible multiplier circuit is designed by using GDI low power technique and is compared with conventional CMOS in terms of area and power. And this done by using Tannar tools.

KEYWORDS: Area, Constant Inputs, Garbage Inputs, Garbage Outputs, Gate Count and Power